FIG. 1

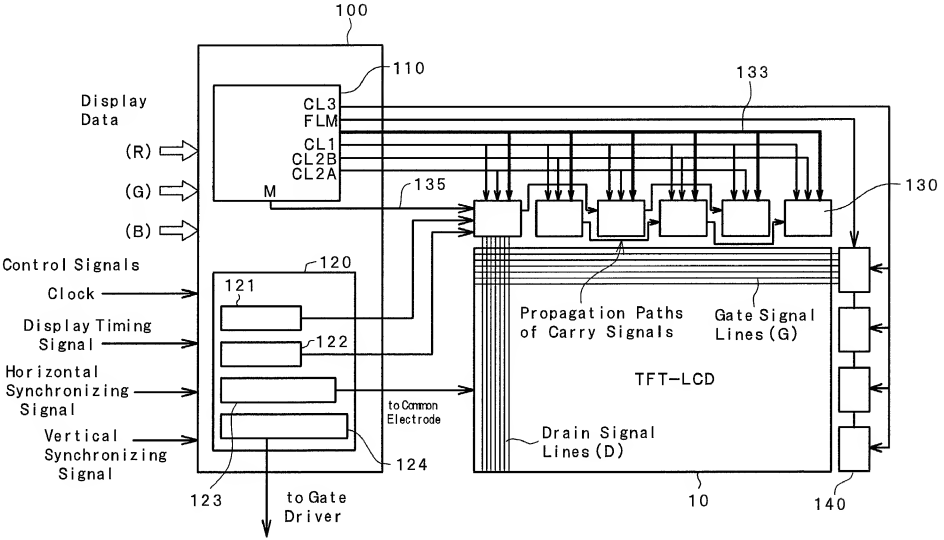

100
110
133
Display Data
(R)
(G)
(B)
CL3
FLM
CL1
CL2B
CL2A
M
135
130
Control Signals
Clock
Display Timing Signal
Horizontal Synchronizing Signal
Vertical Synchronizing Signal
120
121
122
124
123
to Gate Driver
to Common Electrode
Propagation Paths of Carry Signals
Gate Signal Lines (G)
TFT-LCD
Drain Signal Lines (D)
10
140

FIG. 2

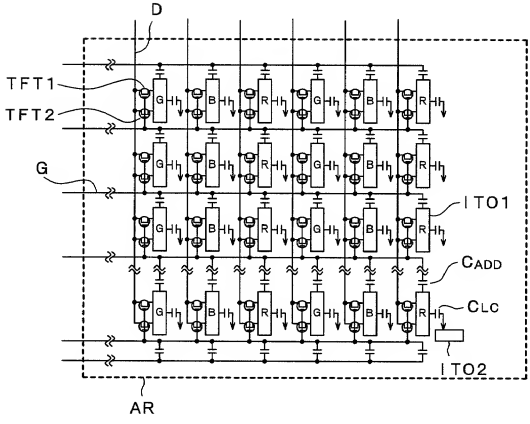


FIG. 3

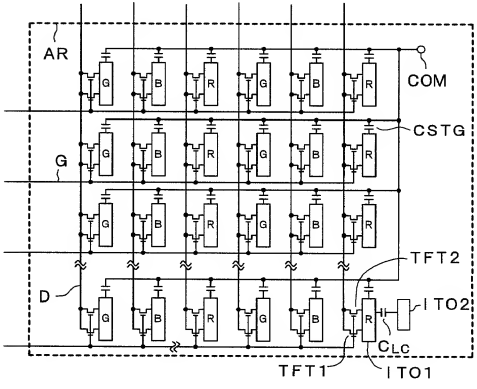


FIG. 4

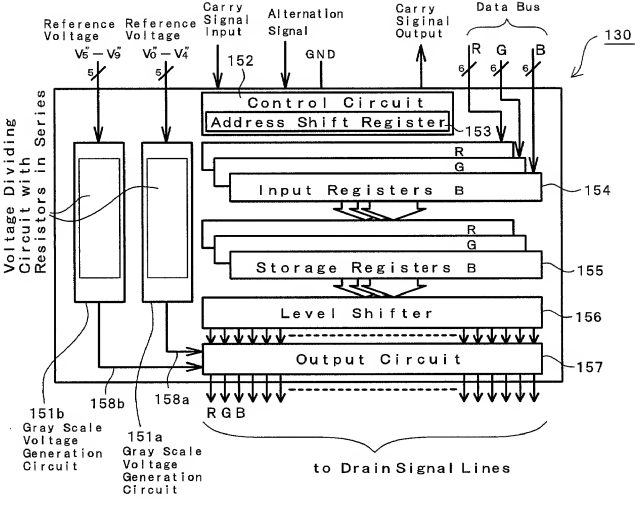

Reference Voltage
V5" – V9"
5
Reference Voltage
V0" – V4"
5
Carry Signal Input
152
Alternation Signal
GND
Carry Signal Output
Data Bus
R G B
6 6 6
130
Control Circuit
Address Shift Register
153
R
G
Input Registers B
154
R
G
Storage Registers B
155
Level Shifter
156
Output Circuit
157
Voltage Dividing Circuit with Resistors in Series
151b
Gray Scale Voltage Generation Circuit
158b
151a
Gray Scale Voltage Generation Circuit
158a
RGB
to Drain Signal Lines

FIG. 5

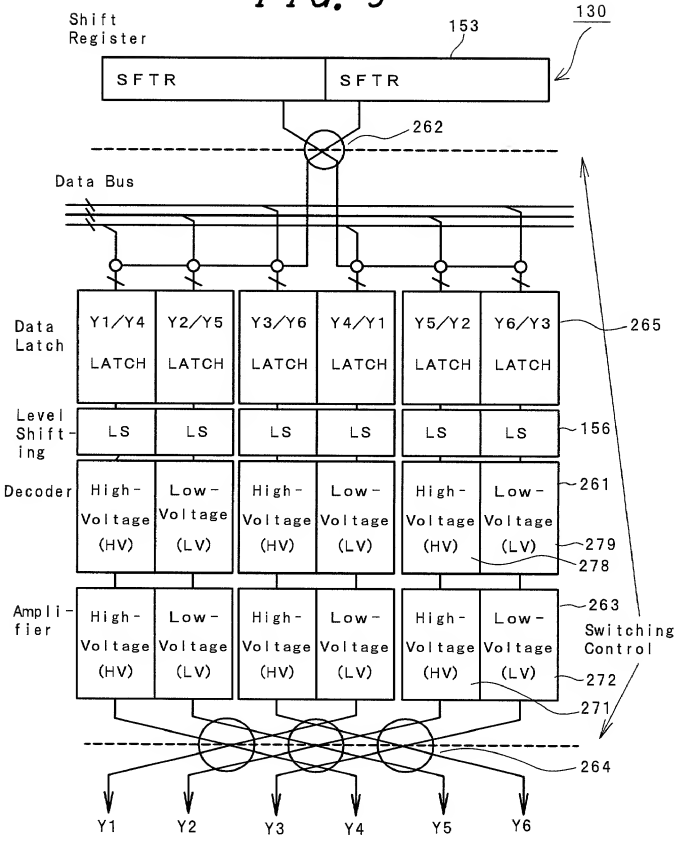

Shift Register
153
130
SFTR
SFTR
262
Data Bus
Data Latch
Y1/Y4 LATCH
Y2/Y5 LATCH
Y3/Y6 LATCH
Y4/Y1 LATCH
Y5/Y2 LATCH
Y6/Y3 LATCH
265
Level Shifting
LS
156
Decoder
High-Voltage (HV)
Low-Voltage (LV)
261
279
278
Amplifier
263
Switching Control
272
271
264
Y1
Y2
Y3
Y4
Y5
Y6

FIG. 6A

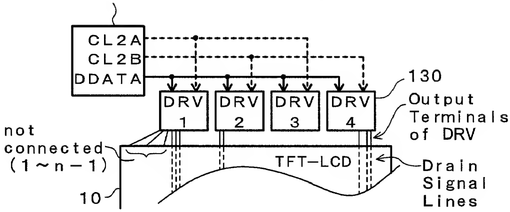


FIG. 6B

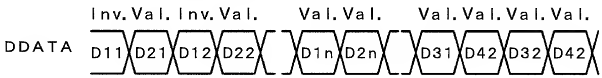


FIG. 6C

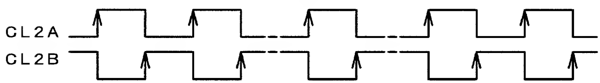


FIG. 7

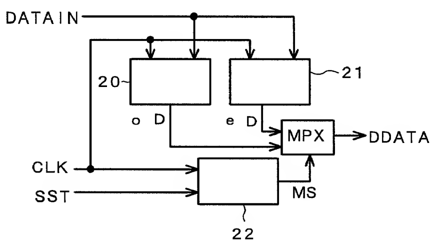


FIG. 8A

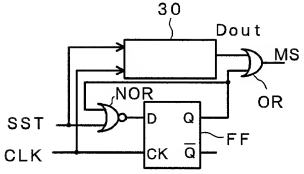


FIG. 8B

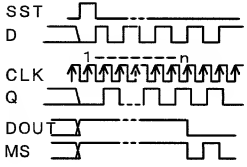


FIG. 9A

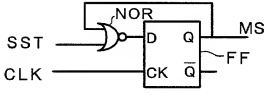


FIG. 9B

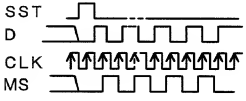


FIG. 10

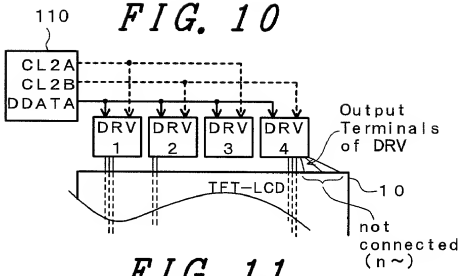


FIG. 11

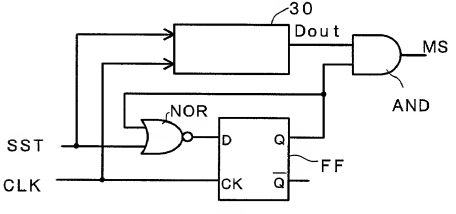


FIG. 12A

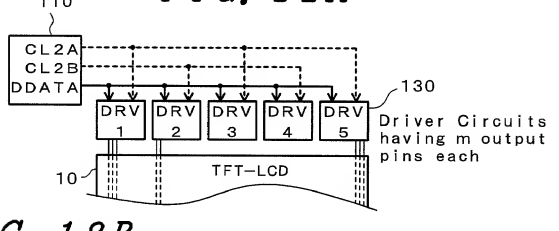


FIG. 12B

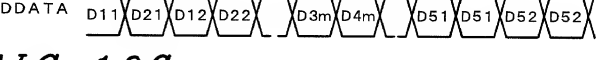


FIG. 12C

FIG. 13

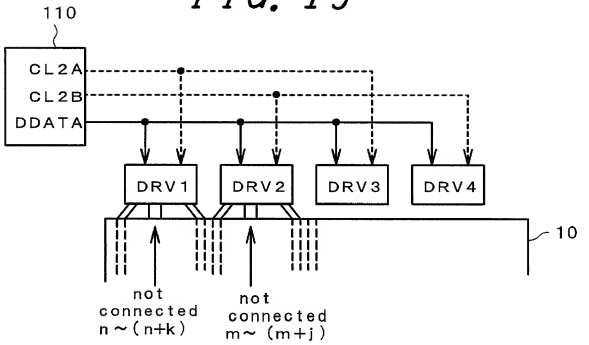

110
CL2A
CL2B
DDATA
DRV1
DRV2
DRV3
DRV4
10
not connected n～(n+k)
not connected m～(m+j)

FIG. 14

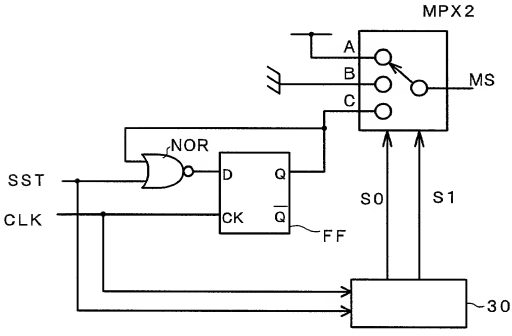
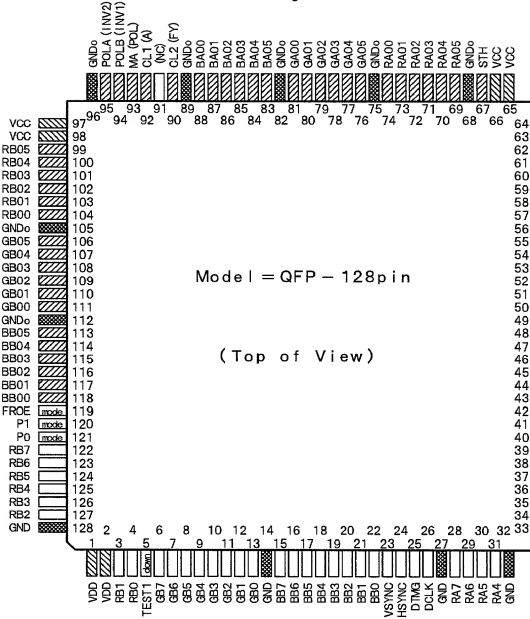

MPX2
A
B
C
MS
NOR
SST
CLK
D
Q
CK
Q
FF
S0
S1
30

FIG. 15



RA[7:0], GA[7:0], BA[7:0] ; For Input Data to First Pixels
RB[7:0], GB[7:0], BB[7:0] ; For Input Data to Second Pixels
DCLK ; Reference Clock (Input)
DTMG ; Display Timing Signal (Input)
HSYNC ; Horizontal Synchronizing Signal (Input)
VSYNC ; Vertical Synchonizing Signal (Input)
PIX ; High − Interface for Second Pixels Input (Mode Pin)
Low − Interface for First Pixels Input

Power Source ; 3. 3[V] (VDD) GND (VSS)
INPUT (CMOS Interface) OUTPUT
INPUT (Pull Up) INPUT (Pull Down)

FIG. 16

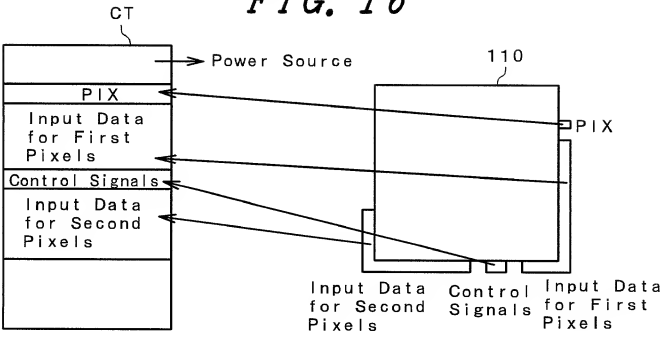

CT
Power Source
110
PIX
Input Data for First Pixels
Control Signals
Input Data for Second Pixels
PIX
Input Data for Second Pixels
Control Signals
Input Data for First Pixels

FIG. 17

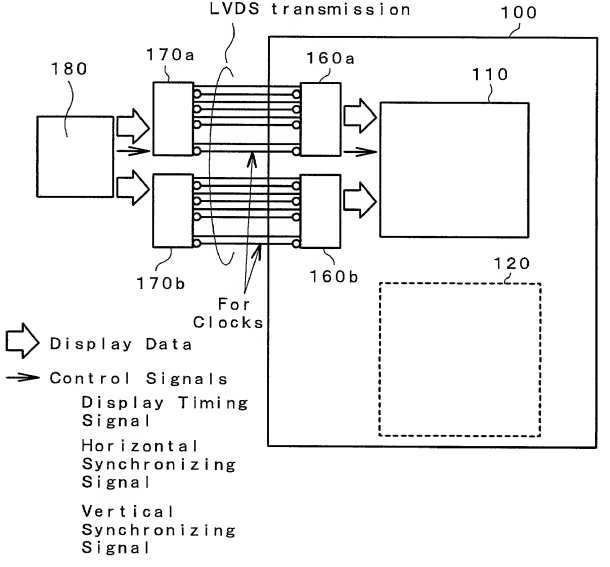

LVDS transmission
100
180
170a
160a
110
170b
160b
120
For Clocks
Display Data
Control Signals
Display Timing Signal
Horizontal Synchronizing Signal
Vertical Synchronizing Signal

FIG. 18

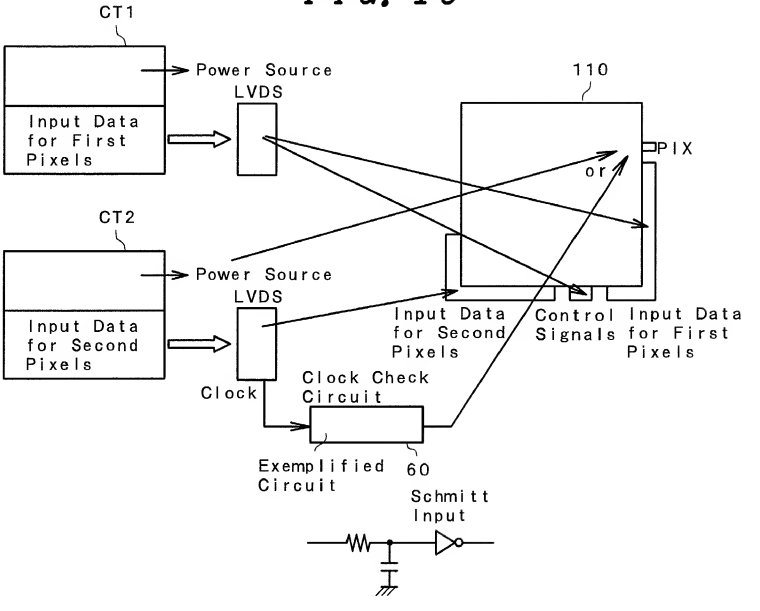

CT1
Power Source
LVDS
Input Data for First Pixels
110
PIX
or
CT2
Power Source
LVDS
Input Data for Second Pixels
Input Data for Second Pixels
Control Signals
Input Data for First Pixels
Clock
Clock Check Circuit
Exemplified Circuit
60
Schmitt Input

FIG. 19A

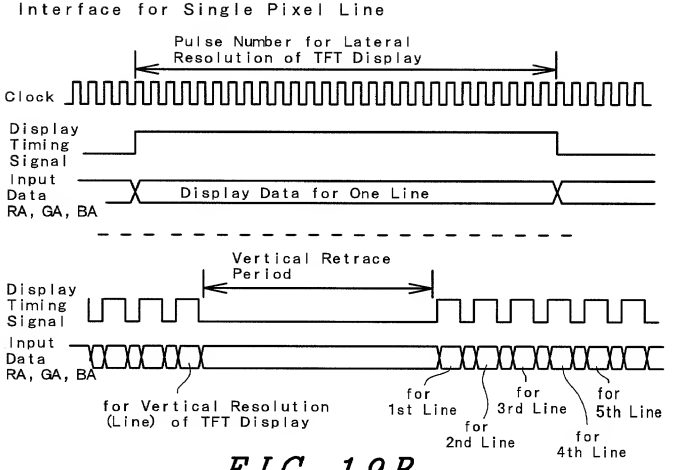
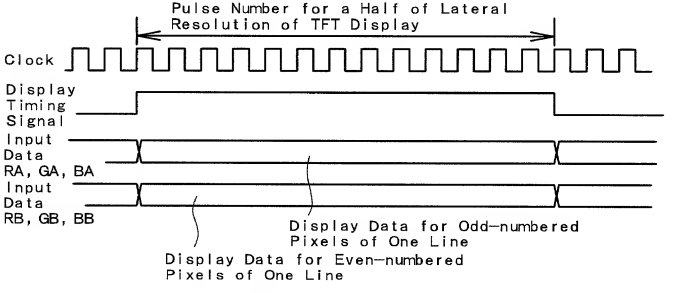


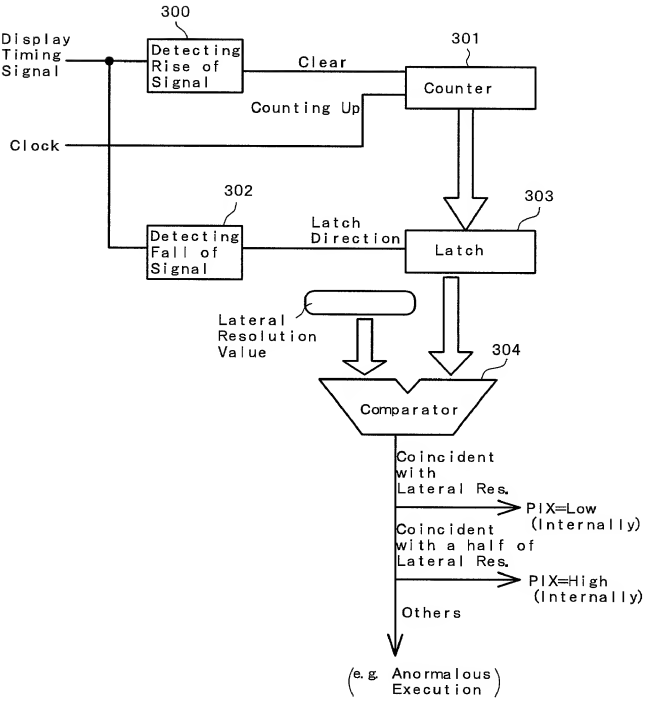
FIG. 19B



Clock period is Two-times Long as that for Single Pixel Line

(Timing for Vertical Retrace Period is same as that for Single Pixel Line)

FIG. 20


300
Display Timing Signal
Detecting Rise of Signal
Clear
301
Counter
Counting Up
Clock
302
303
Latch Direction
Detecting Fall of Signal
Latch
Lateral Resolution Value
304
Comparator
Coincident with Lateral Res.
PIX=Low (Internally)
Coincident with a half of Lateral Res.
PIX=High (Internally)
Others
(e.g. Anormalous Execution)